REMARKS

Claims 63-73 were pending in the present application. Claims 63-68 were rejected and claims 69-73 were allowed in the Office Action dated November 10, 2005. New claims 74 and 75 are added. Reconsideration of claims 63-68 is respectfully requested in light of the arguments presented below.

Claim Rejections under 35 USC §112

Claims 63-68 were rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. With respect to claim 63, the Office Action indicated that two limitations "flash control buffer means for performing data exchange between the flash memory and the interface means" and "access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address" were not supported by the specification.

With respect to the former limitation, it appears that the Office Action identified interface 40 of the present application as "the interface means for exchanging data and addresses with an external system." Because of this identification, the Office Action concluded that FIFOs 519 and 601 "perform the exchange between the microprocessor 21 and the interface 40, not between the flash memory (43) and the interface means (40)," Office Action, paragraph 9, lines 15-17. However, another component that could be considered as the interface means is controller 31 of Figures 1B, 6 and 7 (as originally suggested in the Request for Interference of October 19, 1998). In this case, interface 40 may be considered to be a "flash control buffer means for performing data exchange between the flash memory and the interface means," as it performs data exchange between the flash memory and controller 31. Similarly, interface 227 of Figure 3A performs data exchange between the flash memory and controller 31.

Alternatively, particular portions of controller 31 may be considered to be the interface means of claim 63. Thus the interface means could include one or more of: microprocessor interface port 505, DMA controller 507, output interface 525 and interface input 603 of Figures 6 and 7. In this case, FIFO 519 of Figure 5 and FIFO 601 of Figure 6 may be considered (individually or jointly) to show "a flash control buffer means for performing data exchange between the flash memory and the interface means." Similarly, receiver 515 (previously misidentified as receiver 313) may be considered to show this feature.

The Office Action stated that cache 705 could not be considered as a flash control buffer means because it is "not for reading and writing together, so it does not perform data exchange (two way transferring of data)," page 5, lines 2-3. However, it is submitted that, to be considered "for performing data exchange," cache 705 does not necessarily have to be involved in every stage of data exchange. Cache 705 is clearly involved in data exchange during writing of data as acknowledged in the Office Action. "Cache 705 is used for holding the **data to be write** [sic] to flash memory array 33 only (one way transferring data)," page 5, lines 1-2 (emphasis original). However, as one-way transfer is at least part of an exchange, cache 705 may be considered to be an example of a buffer means for performing data exchange.

Alternatively, cache system 701of Figure 8; or a portion thereof, may be considered as a "flash control buffer means for performing data exchange," instead of considering only cache 705. In this case, transfer of data in both directions is performed as indicated by the "Data" line between host interface 703 and flash memory array 33 and described at page 23, lines 31-35. Thus, cache system 701 supports this limitation even if the limitation is given the narrow meaning that the means for performing data exchange must be involved in both reading and writing of data.

Where either cache 705 or cache system 701 (or a portion thereof) is considered as the buffer means, host interface 703 may be considered as at least a portion of an "interface means for exchanging data and addresses with an external system" of claim 63. Thus, either cache 705 or cache system 701 may be considered to perform "data exchange between the flash memory and the interface means" of claim 63.

With respect to the "access means for converting" limitation, at least two examples are given in the specification. One example of "access means for converting" of claim 63 is provided by mapping of defective sectors. "When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector." Page 23, lines 17-19. The Office Action indicated that this was not considered as "access means for converting" of claim 63 because "**such means does not convert <u>any</u> sector address when there is no defective sector**," page 7, lines 19-20 (emphasis original). However, the relevance of this statement is not understood. Claim 63 merely requires "access means for converting **<u>a</u>** sector address," (emphasis added). The Office Action appears to acknowledge that conversion does occur for a defective sector. "The mapping happens only when the defective sector exists,"

Office Action, page 7, lines 2-3. It is submitted that a defective sector is nevertheless a sector. Therefore, the address of a defective sector is an example of "a sector address" of claim 63. The Office Action appears to read "converting a sector address" of claim 63 as, "converting any" or "converting all" sector addresses. "'Access means for converting...' in claim 63 will convert **any address, no matter that address is a defective address or not**." Office Action, page 7, lines 11-14 (emphasis original). However, this limitation does not appear in the plain language of claim 63 and it is not seen how the claim term "a sector address" is given the meaning "any address, no matter that address is a defective address or not" in this context. If this basis of rejection is maintained, it is requested that further explanation be given as to why the word "a" is interpreted in this way here.

Another example of an "access means for converting" is decoding an address to access the memory. Figure 3A shows decoder 233. "Address information is captured by an address register 231 and is decoded by an address decoder 233," page 10, lines 9-11. The Office Action indicated that decoding was not considered an example of converting. However, this interpretation of the word "converting" is not understood. The operation carried out by decoder 233 appears to be an example of conversion. "In order to select the sector 211 for erase, the controller sends the address of the sector 211 to the circuit 220. The address is decoded in line 235 and is used in combination with a set erase enable signal in bus 237 to set an output 239 of the register 221 to HIGH." Page 10, lines 12-17. Thus, an address for sector 211 is received by decoder 233, which applies a signal to line 235 in response. In this way, decoder 233 converts an address that identifies a sector into a signal on a specific line. The Office Action, in explaining the term "converts," states, "For example, converting a physical address to a logical address means changing the address from one form (physical form) to another form (logical form)." Page 6, lines 13-15. It is submitted that decoder 233 also changes an address from one form (address of sector 211 from register 231) to another form (signal on line 235). Thus, if converting is defined as effecting a change from one form to another, the above example is believed to provide an example of such conversion.

With respect to claim 64, the Office Action stated, "if there are few defective memory cells, the defect mapping of the whole sector does not happen," page 8, lines 8-9. The significance of this statement is not understood. Claim 64 only requires that each block comprise "an area for storing an address of another block," not that a block address must always be stored

in such an area. It is submitted that even where a block does not store an address of another block, it may have an area for storing an address of another block. Sector 401 of Figure 5 has spare portion 405. Whether spare portion 405 actually stores defect data or not, the area may be considered to be for storage of such data. The Office Action stated, "The address of the replace [sic] sector is stored in another memory maintained by the controller." Page 8, lines 11-12. However, in another embodiment a defect pointer for a substitute sector is maintained in a defective sector. "When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector. The defect pointer for the linked sectors may be stored in a sector defect map. The sector defect map may be located in the original defective sector if its spare area is sufficiently defect-free." Page 23, lines 19-23 (emphasis added). Thus, a defective sector contains a defect map, which includes a pointer to a replacement sector.

Claim 66 is submitted to be supported similarly to claim 64.

Claim 65 is amended to replace "logical block address" with "block address." Claim 65 as amended is believed to be fully supported. In particular, the specification states, "In other devices... the memory is divided into blocks (or sectors) that are each separately erasable." Page 8, lines 27-29. "When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector. The defect pointer for the linked sectors may be stored in a sector defect map." Page 23, lines 17-21. Thus, a defect map contains a pointer for a substitute block (or sector).

Claims 74 and 75 are added by this amendment. Claim 74 is similar to claim 63 but with claim language that is believed to overcome certain rejections made with respect to claim 74. In particular, claim 74 recites, "a flash control buffer for performing data transfer." The term "transfer" is believed to apply to apply to one-way or two-way movement of data. Claim 74 is submitted to be supported similarly to claim 63. Claim 75 is supported throughout the specification, in particular by page 23, lines 12 - page 24, line 2.

CONCLUSION

In view of the amendments and remarks contained herein, it is believed that all claims are fully supported by the specification and it is requested that all rejections be withdrawn and an interference be declared as previously requested. However, if the Examiner is aware of any

additional matters that should be discussed, a call to the undersigned attorney at: (415) 318-1160 would be appreciated.

Respectfully submitted,

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Gerald P. Parsons
Reg. No. 24,486

Date

PARSONS HSUE & DE RUNTZ LLP
595 Market Street, Suite 1900
San Francisco, CA 94105
(415) 318-1160 (main)
(415) 318-1163 (direct)
(415) 693-0194 (fax)